Who is Steve Casselman?

PRINCIPAL INVESTIGATORS (NAME AND TITLE)
Steven M. Casselman

TITLE OF PROJECT
A Fully Programmable Reconfigurable Hardware Architecture Supercomputer.

TOPIC TITLE	TOPIC NUMBER
NEW COMPUTING DEVICES	15 D

TECHNICAL ABSTRACT (LIMIT TO 200 WORDS)

The research proposed is investigation of a new approach into the area of supercomputing. With the advent of the programmable gate-array, [1] the possibility of mapping a software program directly into a large number of such devices implies a significant advance in the area of supercomputing. This ability to repeatably map software directly into a fully reconfigurable hardware architecture will minimize many of the problems facing conventional and parallel supercomputing such as memory fetch, microcode memory fetch, and sequencer decoding delay.

The research to be done will be two-fold:

1) Study the topology of the interconnection of arrays to find a way to allow a continuous plane of arrays to be created.

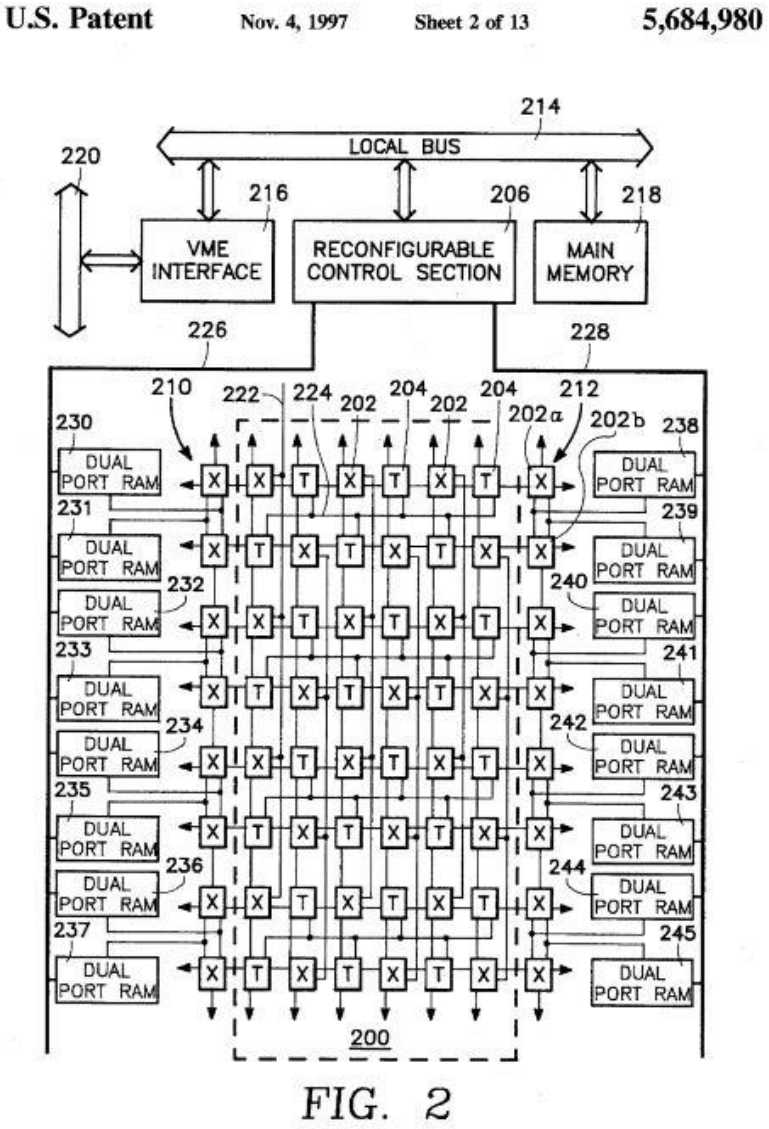
2) Write a compiler that will map a source code file into the proper binary format needed by the arrays.

1987 SBIR

KEY WORDS TO IDENTIFY RESEARCH OR TECHNOLOGY (8 MAXIMUM)
Supercomputer, Reconfigurable Hardware.

POTENTIAL COMMERCIAL APPLICATIONS OF THE RESEARCH
Commercial applications range from use in highly recursive mathematical and physical problems to high speed simulation of large systems.

Who is Steve Casselman?



My first patent was Filed in 1992 Granted in 1997

HOTWRIGHT FPGA ACCELERATION

Who is Steve Casselman?

Stacked wafers of FPGA fabric.

Manufacturing flaws are put in a purge map

Connected via fiber optics.

A better vision today than in 1991!

MRL COMPUTERS TURN ALGORITHMS INTO HARDWARE

When adding processors to massively parallel processing (MPP) systems, there is never a time when, by doubling the number of processors, you more than double the throughput of the system. That is loosely known as Amdahl's law or (if there is a 1:1 speedup) the law of perfect speedup.

A computer architecture that could violate that law would be more than "perfect"—the computer-science equivalent of breaking the speed-of-light barrier in physics. Yet there is an architecture that does precisely that: massively reconfigurable logic (MRL).

An MRL computer can reconfigure its internal logic completely, in real-time, to implement an algorithm in hardware. It does so via field-programmable gate arrays. Downloading a file to the FPGAs rearranges the logic and routing resources inside to implement a hardware design.

The Supercomputing Research Center (SRC, Bowie, Md.) has already used the technique to build a machine that outperforms the Cray 2 by 330 times, operating on DNA-sequence comparisons.

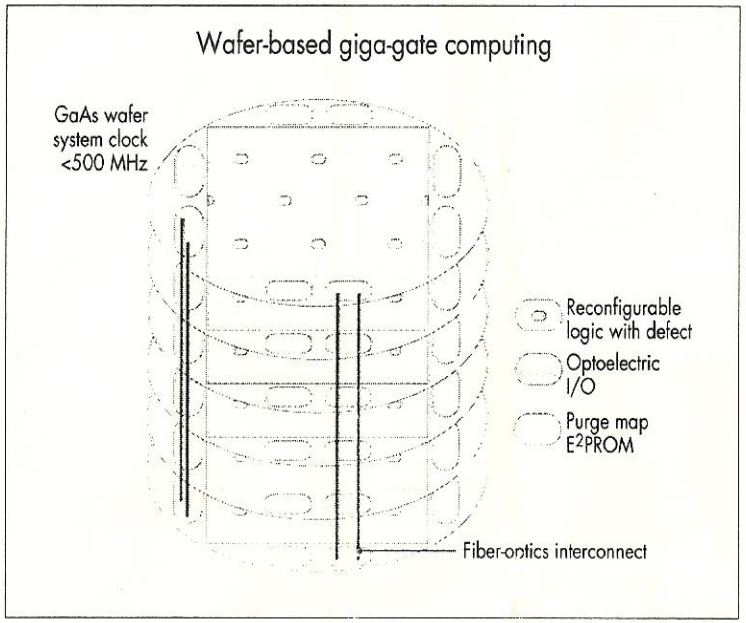
Our version of an MRL computer, the Virtual Computer, is a single-board desktop machine with more than 500,000 gates of reconfigurable logic.

Since MRL systems use commercial, off-the-shelf parts, they are cheap, at $125,000. And with no moving parts, they can be offered with multiyear guarantees and reasonable repair cost estimates after that.

If a single transistor goes bad in a microprocessor, the whole chip is bad. In an MRL system, by contrast, a bad spot can be marked as not usable, much as in a hard disk's purge map. That will lead to the first efficient use of wafer-scale integration in which every wafer can be used.

Supercomputers in the year 2000 will be more open, more versatile and more reconfigurable than anyone can imagine at this time. Our vision for the future of computing is MRL-based Virtual Computers capable of 10^{15} operations/second at a cost of under $500,000. ■

—By Steven Casselman, president, Virtual Computer Corp. (Reseda, Calif.).



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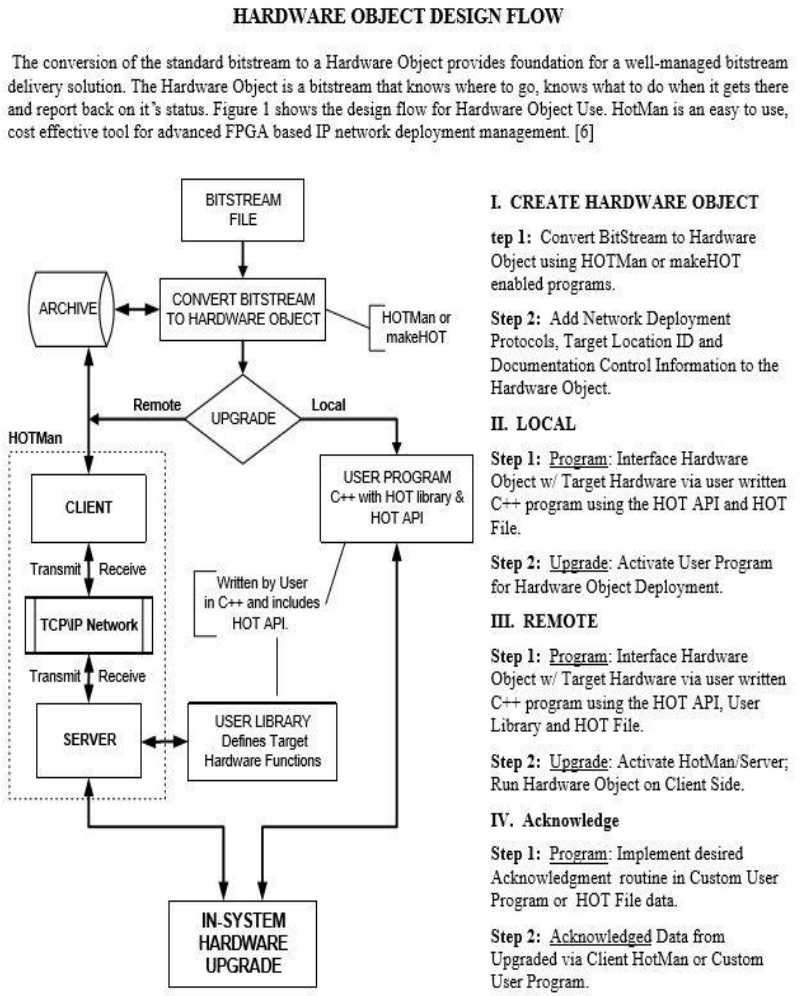

HARDWARE OBJECT DESIGN FLOW

The conversion of the standard bitstream to a Hardware Object provides foundation for a well-managed bitstream delivery solution. The Hardware Object is a bitstream that knows where to go, knows what to do when it gets there and report back on it's status. Figure 1 shows the design flow for Hardware Object Use. HotMan is an easy to use, cost effective tool for advanced FPGA based IP network deployment management. [6]

I. CREATE HARDWARE OBJECT

tep 1: Convert BitStream to Hardware Object using HOTMan or makeHOT enabled programs.

Step 2: Add Network Deployment Protocols, Target Location ID and Documentation Control Information to the Hardware Object.

II. LOCAL

Step 1: Program: Interface Hardware Object w/ Target Hardware via user written C++ program using the HOT API and HOT File.

Step 2: Upgrade: Activate User Program for Hardware Object Deployment.

III. REMOTE

Step 1: Program: Interface Hardware Object w/ Target Hardware via user written C++ program using the HOT API, User Library and HOT File.

Step 2: Upgrade: Activate HotMan/Server; Run Hardware Object on Client Side.

IV. Acknowledge

Step 1: Program: Implement desired Acknowledgment routine in Custom User Program or HOT File data.

Step 2: Acknowledged Data from Upgraded via Client HotMan or Custom User Program.

Hardware Object Technology

H.O.T.

- Takes a FPGA bitstream and turns it into a plain vanilla static array
- Compiles on all OSes
- The array is a field in a C++ object with methods to:
  - Configure
  - Write to the hardware
  - Read from the hardware
  - Debug the hardware
- Works with partial configurations

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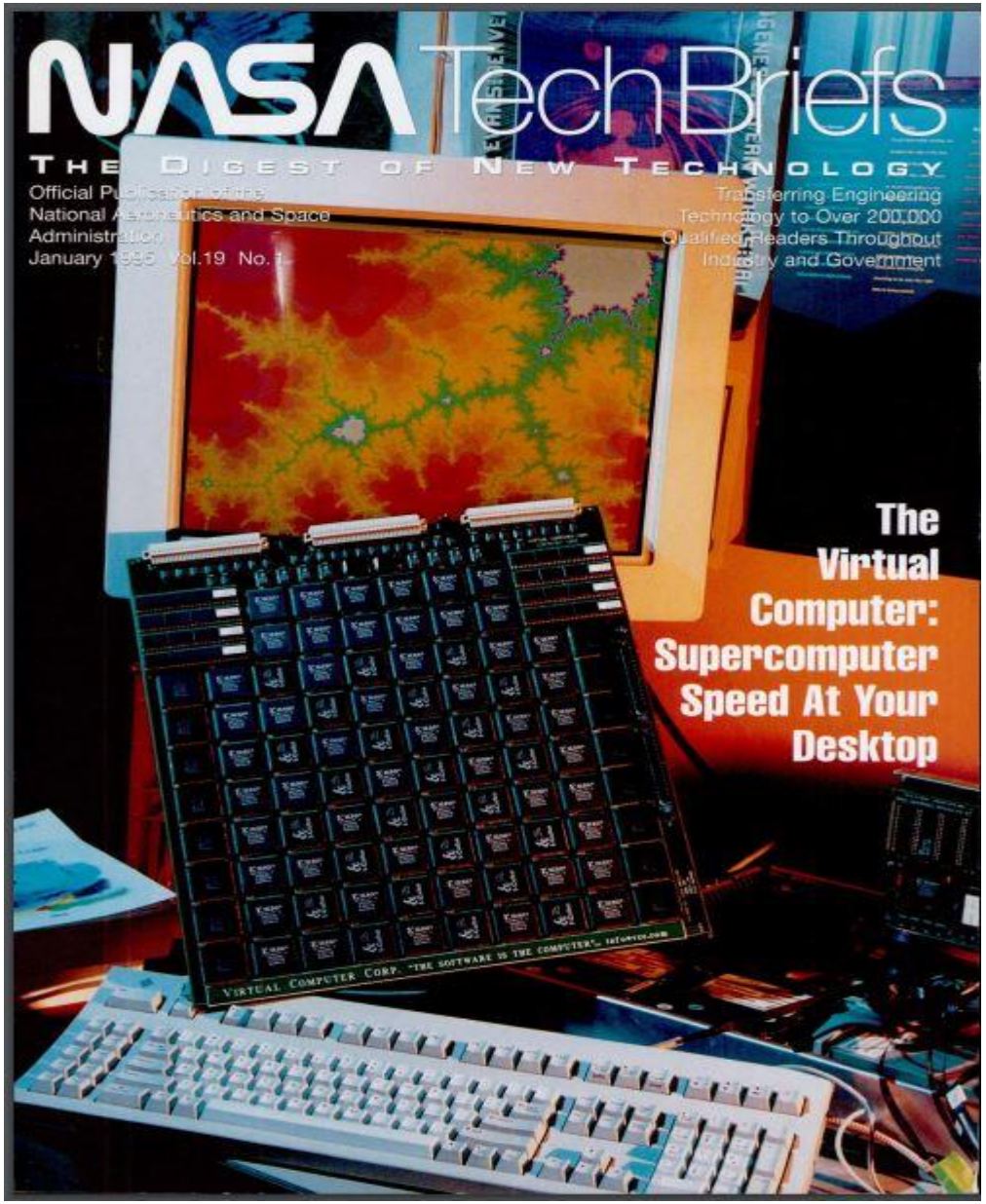

Virtual Computer Corporation (VCC), Reseda, CA, developed its award-winning Virtual Computer™ for the US Naval Surface Warfare Department in 1991. The device is one of a new class of computing machine called reconfigurable hardware. This class employs massively reconfigurable, or programmable, logic, blurring the line between hardware and software.

The technology solves the problem of Amdahl's law, which limits performance improvements on hardware scale-ups:

For more information about the 1995 SBIR Technology of the Year competition, contact Wayne Pierce, Technology Utilization Foundation, 41 East 42nd St., Suite 921, New York, NY 10017. Tel: 212-490-3999; Fax: 212-986-7864.

First SBIR Technology of the year, 1995

HOTWRIGHT FPGA ACCELERATION

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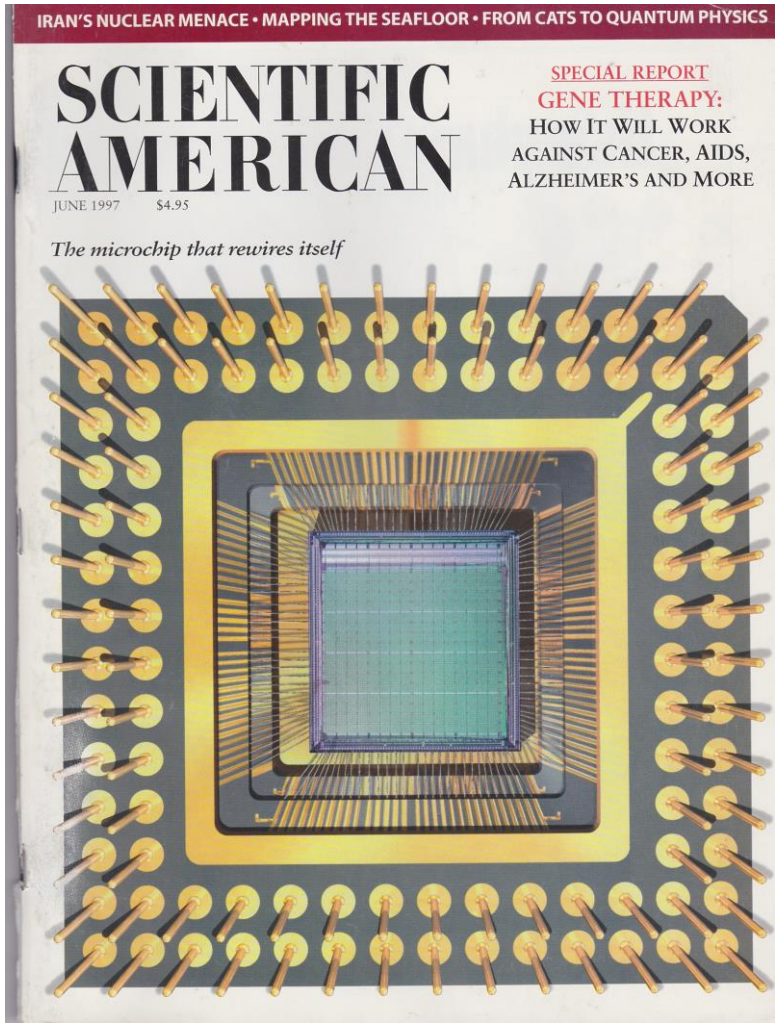


In a Scientific American article DARPA promised to invent the future.

We made a deal with the distributor where they sourced all the components for the board

We then packaged the board with our software, and they stocked and sold all systems

HOTWRIGHT FPGA ACCELERATION

Who is Steve Casselman?

In the same issue of Scientific American, we offered the future for sale

Incorporating customer satisfaction

The browser implements the customer satisfaction specifiers. Developers modify the browser so that it can collect data about clicks to select a page, cache a page, purchase from a page, and so on. Since many successful browsers (such as Netscape) are now public domain, this is not a problem. Even privately owned companies such as Microsoft will likely permit ISPs to upgrade their proprietary browsers if customers demand these customer satisfaction specifiers. The modified browser collects this data for every Web site hosted at the ISP.

Tracking customer behavior

Another ingredient we can include is customer behavior, which lets the profile be changeable and traceable in time. By analyzing a customer's past actions, we can extrapolate to predict new actions. This allows better efficiency of the entire product.

Developers can design various algorithms to implement approaches that are more or less sophisticated than the one presented in this scenario. Real-market experiments can show the advantages and drawbacks of these different algo-

Reconfigurable chips allow user-tailored Internet searches. The first step is collecting customer data. After that, the search engine leads the way.

Behavioral Search and Targeting July 2000

FPGAs let you think out of the box

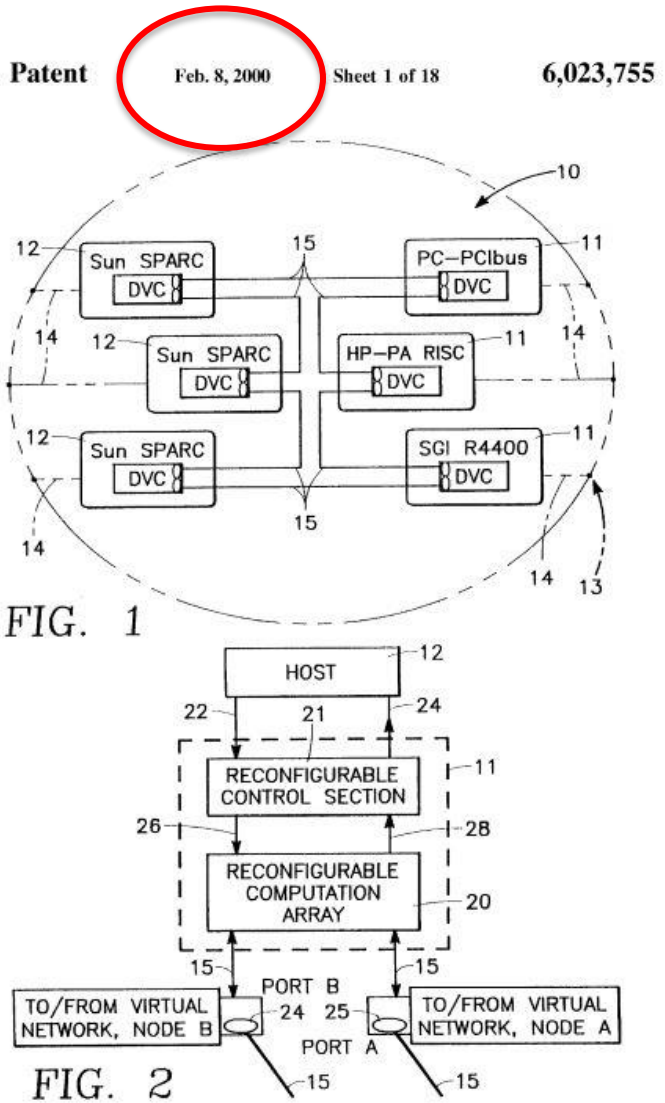
Who is Steve Casselman?

Distributed Virtual Computer (DVC)

The DVC allowed you to build system of directly connected FPGAs

Round trip latency was sub 2 microseconds a world record at the time.

Microsoft now uses this in all their new Data Center Clusters



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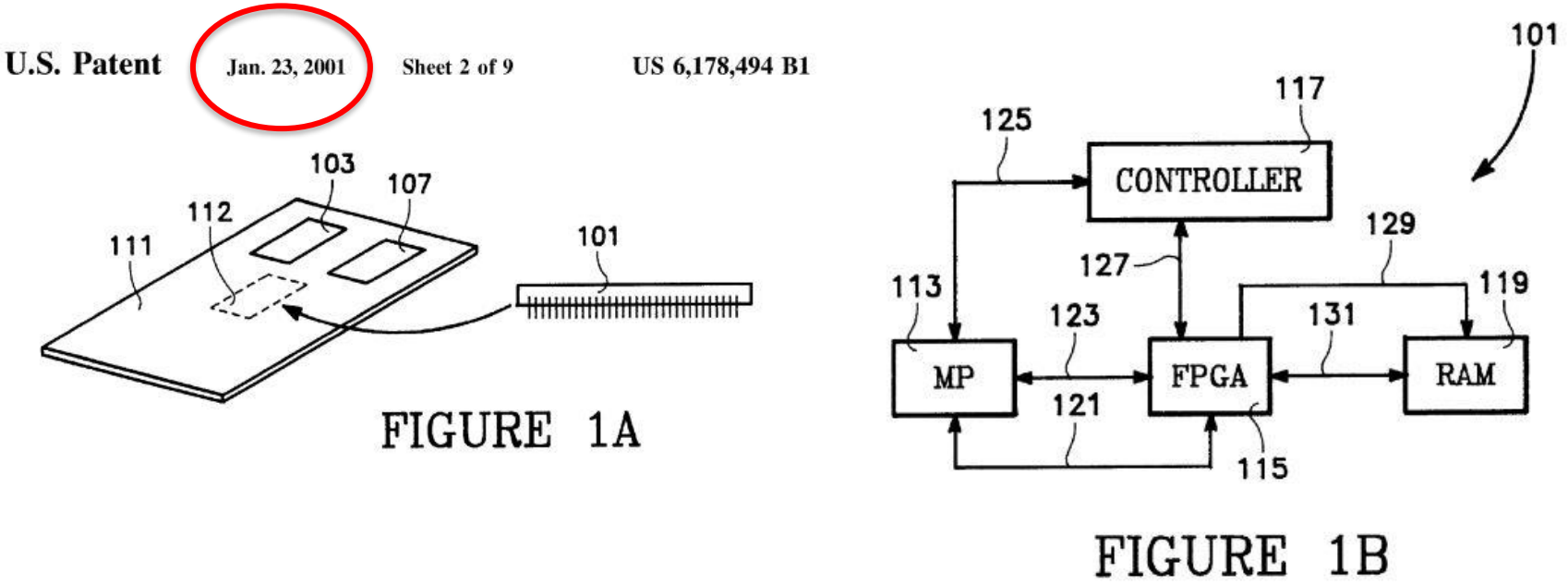

This is Intel's Current Plan

Who is Steve Casselman?

(12) **United States Patent**
Casselman

(10) **Patent No.: US 6,289,440 B1**
(45) **Date of Patent: Sep. 11, 2001**

(54) **VIRTUAL COMPUTER OF PLURAL FPG'S SUCCESSIVELY RECONFIGURED IN RESPONSE TO A SUCCESSION OF INPUTS**

(75) Inventor: **Steven Casselman**, Woodland Hills, CA (US)

(73) Assignee: **Virtual Computer Corporation**, Reseda, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/353,522**

(22) Filed: **Jul. 14, 1999**

Related U.S. Application Data

(63) Continuation of application No. 09/120,958, filed on Jul. 22, 1998, now Pat. No. 6,023,755, which is a continuation-in-part of application No. 08/685,158, filed on Jul. 23, 1996, now Pat. No. 5,684,980, which is a continuation of application No. 08/357,059, filed on Dec. 14, 1994, now abandoned, which is a continuation of application No. 07/922,167, filed on Jul. 29, 1992, now abandoned.

(51) **Int. Cl.**[7] **G06F 9/30**
(52) **U.S. Cl.** **712/227**; 712/226; 712/209
(58) **Field of Search** 712/209, 227, 712/226

(56) **References Cited**

PUBLICATIONS

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Dillien, Paul C., *Adaptive Hardware Becomes a Reality using Electrically Reconfigurable Arrays* (ERAs), IEE Colloquium on User-Configurable Logic—Technology and Applications, Dec. 1990, pp. 2/1 to 2/5.*

Dillien, Paul C., Electrically reconfigurable arrays–ERAs, IEE Colloquium on New Directions in VLSI Design, 1989, pp. 6/1 to 6/6.*

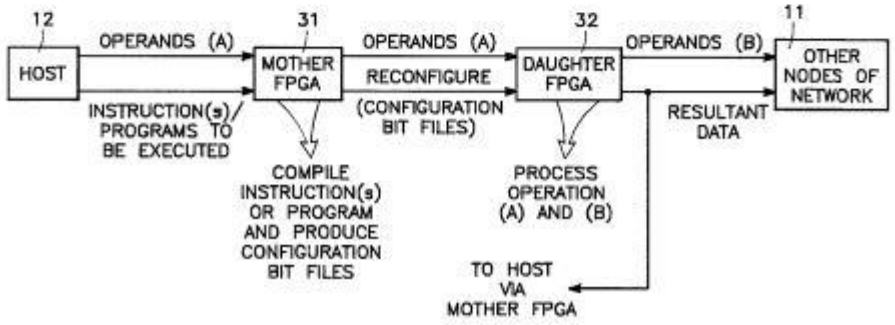
* cited by examiner

Primary Examiner—Richard L. Ellis
(74) *Attorney, Agent, or Firm*—Michaelson & Wallace

(57) **ABSTRACT**

A virtual network consists of many distributed virtual computers interconnected over a communication network of individual links, such as optical fibers or electrical conductors, for example. Each distributed virtual computer has at least two ports connected over respective links to other respective distributed virtual computers on the network. Each distributed virtual computer is connected to or resident within its own host, each host typically being a conventional computer such as a personal computer or a work station, for example, although at least one of the hosts may itself be another virtual computer. Each distributed virtual computer has reconfigurable logic elements such as an FPGA or an array of FPGAs.

9 Claims, 18 Drawing Sheets



The Tech bubble pops, and Virtual Computer Corporation goes insolvent

I personally took on the debt of the company so the technology could be moved to a clean corporation in 2004

DRC Computer Company moved to the silicon valley and started raising money

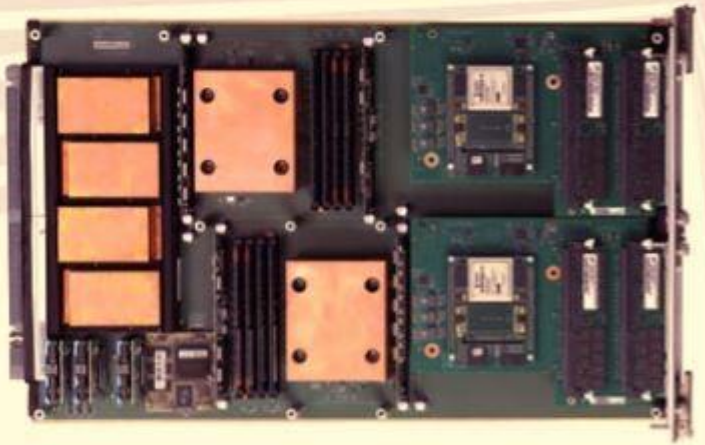
I took a CTO back seat to a fungible CEO and we raised $12 million over the next 5 years

HOTWRIGHT FPGA ACCELERATION

Who is Steve Casselman?

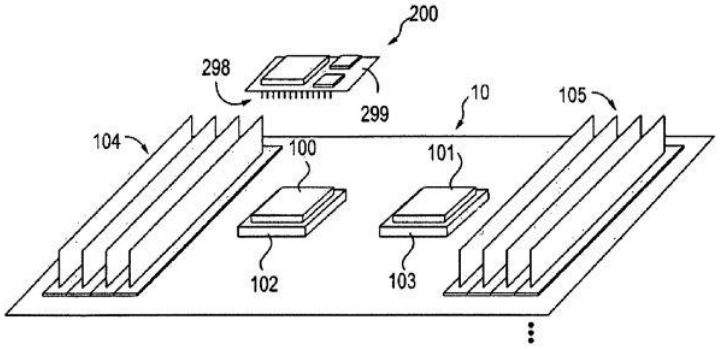
The Cray XR1 Reconfigurable Processing Blade, compatible with existing Cray XT3™ and Cray XT4™ systems as well as new Cray XT5$_h$™ systems, offers users orders of magnitude speedup on select applications as well as large potential savings in cooling and space. Building on the established track record of the Cray XT™ product line and the reconfigurable computing capability in the Cray XD1™ system, the Cray XR1 reconfigurable processing blade is the first product on the market capable of massively parallel reconfigurable computing.

Cray XR1 Reconfigurable Processing Blade



High Bandwidth, Direct Connect Architecture

A Cray XR1 reconfigurable blade has two nodes, consisting of a single AMD Opteron™ processor tightly coupled with two DRC Computer's reconfigurable processing units (RPUs). This connection is made directly with HyperTransport™, which ensures that RPUs are tightly coupled with AMD Opterons, delivering low-latency and high-bandwidth communication between the processing elements.



FPGA in the processor socket filed in 2007

OEMed by Cray

Bought by the Australian and New Zealand secret services.

HOTWRIGHT FPGA ACCELERATION

Who is Steve Casselman?

June 10, 2009

Acquisition of the Week: DRC Computer Corporation

by Michael Feldman

The acquisition beat goes on. DRC Computer Corporation, a maker of FPGA-based coprocessor accelerators, has been bought up by Security First, a company that offers data security/integrity products. The acquisition was closed last Friday and announced on Monday. Financial terms of the deal were not disclosed.

DRC has been around since 2004 and started shipping its FPGA-based reconfigurable coprocessors in 2006. The company is on its 3rd generation hardware. The latest DRC module, Accelium, uses Xilinx Virtex-5 FPGAs and plugs into a standard AMD Opteron Socket F slot, using HyperTransport to provide very low latency data transfers between the FPGA, the CPU, and on-board memory. The ability to reconfigure the FPGA hardware and fast on-board communication are the keys to its high performance as a coprocessor. Compared to software running on a CPU, an FPGA-based kernel can run hundreds of times faster.

The main application area for these coprocessors is HPC acceleration, where the highly parallel nature of the FPGA architecture makes it especially suitable. But because of the non-traditional programming model, which entails special development tools and languages, FPGAs never really took off in a big way in HPC. Despite that, DRC has been quietly gathering customers, and adding application expertise and software tools. In general, DRC has focused its efforts on financial services, security, Web companies and biomedical markets.

DRC received its startup funding from TopSpin Partners and Capital Valley Ventures (now Wavepoint Ventures). In April 2008, the company was voted the top business seeking funding in the VC Panel and Business Plan Contest at the Data Protection Summit. Despite that accolade, when it came time to do its B round of funding this year, investors came up short. According to DRC CEO and co-founder Larry Laurich, they got "tantalizingly close" to nailing down the money, but couldn't close the deal. That's not too surprising considering that a number of HPC vendors have succumbed to a shortfall in venture capital this year, the latest victims being SiCortex and Woven Systems.

The Great Recession forced the Acquisition of DRC, but we soldiered on refusing to go away

DRC is still in business today

Who is Steve Casselman?

DRC Computer Establishes Stunning Genomics World Record

First Highly Scalable Gene Sequence Analysis Appliance Delivering Multi-Trillion Cell Updates per Second Running on Microsoft Windows HPC Server 2008 R2

February 01, 2011 07:30 AM Eastern Standard Time

SUNNYVALE, Calif.--(BUSINESS WIRE)--DRC Computer Corporation (DRC), the leading innovator of dynamically reconfigurable processors, announces that it has achieved 9.4 trillion cell updates per second (TCUPS) running the Smith-Waterman algorithm with Affine gap model on the latest DRC Accelium coprocessors. Now medical researchers, pharmacologists and DNA forensic experts can more effectively and rapidly analyze human gene sequences to identify medical conditions, build new treatments and complete criminal investigations.

CTO vision

Be the best in the world at some algorithm!

EDN NETWORK

10 Things I saw at IDF2014

Ransom Stephens - September 15, 2014

7. Not exactly Silicon Photonics—but Steve Casselman!

Altera had a 100 Gbit/s Ethernet system up and running: four wavelengths of 25 Gbits/s optical signals on an 11 km single-mode fiber. That alone wouldn't have made my top 10 because the regions of the show floor partitioned as "Silicon Photonics" didn't have anything that I think qualifies as genuine silicon photonics; plenty of great optical transceivers and cutting edge fiber optics, but no etched optical waveguides or chip-to-chip data signaling. Transceivers, silicon photonics does not make.

I was personally the 7th most interesting thing of the Intel developers form in 2014

What brought Altera's 100 GbE demo into my top 10 was Steve Casselman. Steve's an FPGA veteran who has been working on field programmable devices since the 1980s and he described how FPGAs (field programmable gate arrays), microprocessors, and ASICs are merging into a single chip. I know, we've seen it coming, but now they've got FPGAs running on FPGAs to the point where, from the perspective of embedded programmers, they're indistinguishable from microprocessors.

HOTWRIGHT FPGA ACCELERATION

Founder & CEO – Steve Casselman

sc@hotwright.com

- Steve Casselman invented reconfigurable computing in 1987 when he won his first SBIR contract to build a supercomputer out of FPGAs
- Steve has been a founder and C level executive for over 25 years
- Steve helped raise $12 million for DRC Computer and oversaw DRC's acquisition by its largest customer
- As founder and CEO of Virtual Computer Corporation Steve patented:
  - FPGA + CPU in the processor socket
  - runtime generation of bitstreams
  - distributed reconfigurable computer
  - 12 patents all in reconfigurable computing
- Xilinx OEMed the VCC PCI board
- Founder and CTO of DRC Computer Steve got Cray to OEM DRC equipment.
- Steve has been on many international IEEE and ACM conference program committees:

Last word about Steve Casselman and the future

I'm a leader and visionary and all my work has prepared me to help lead this technological shift in the data center.

Both Microsoft, AMD, and Intel have come to the same conclusion I did over 30 years ago.

FPGAs will dominate the Data Center in the next 5 years and Hotwright Inc. plans to be in the eye of the storm.